STUDY OF MULTI BAND HYSTERESIS MODULATION STRATEGYFOR MULTILEVEL INVERTERS

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ABSTRACT

This paper deals with the multiband hysteresis control technique which tracks the desired reference current and provide desired voltage and current waveform with less distortion. Cascaded H bridge multilevel inverter and Neutral point clamped multilevel inverter is used because of its high power and medium power applications. Multiband tracks the desired reference current and is used for evaluating the performance of multilevel inverters. This control technique is based on time domain formulation. The efficiency of the controller in reducing total harmonic distortions and switching losses based on the instantaneous switching frequency, system parameters and number of levels is studied. The simulation results are obtained for five level cascaded H bridge inverters and Neutral point clamped multilevel inverter.

INDEX TERMS: Multilevel inverters, Multiband hysteresis control technique.

1. INTRODUCTION

Multilevel inverters has gained its importance due to wide range of medium and high power applications. Staircase AC voltage is the output of multilevel inverters depending on the levels the staircase levels may increase. The other features of this inverters include improved harmonic spectrum, low switching losses and low voltage stress on all power semiconductor devices used in the inverter. The simplicity and modularity of Cascaded H bridge inverters and Neutral Point Clamped Inverter has increased its significance. The term multilevel was begun with three level converter where a series of single full bridge inverters with several low dc voltages are connected in series to perform power conversion. To achieve high voltage at the output multiple dc sources are used however the rated voltage of power semiconductor switches depends only on the rating of the dc voltage sources to which they are connected. The Multiband hysteresis Modulation Technique has been used by the multilevel inverters for tracking the current and comparator is used to compare it with reference current and error is tracked within the band limit . Batteries, capacitors and renewable energy sources are used for multiple dc sources. Photovoltaic, wind, fuels cells used in combination with multilevel inverter are used for high power application.

2. MULTILEVEL INVERTER

The basic building block for cascaded H bridge inverter is shown in fig 1a.For a N level cascaded H bridge inverter separate DC source is connected to single phase full bridge and H-bridge inverter. Each inverter bridge is cascaded depending on the levels required and generates three output voltage levels +Vdc, 0,-Vdc for a three level inverter using different combination of switches S1,S2,….Sn.
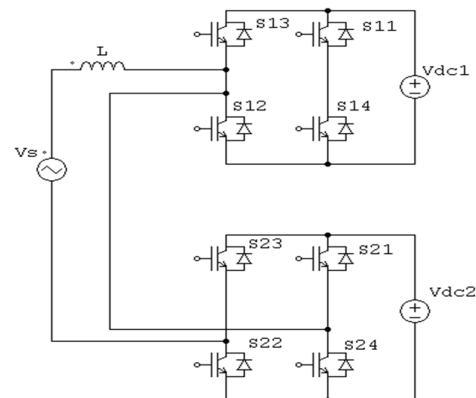

Fig 1.a:Cascaded H bridge 5 level inverter.

The switching states for Cascaded H bridge inverter is given in table 1

Switching States:

Table 1:Switching states for CMLI

S1	S2	S3	S4	S5	S6	S7	S8	V0
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	V1
1	0	0	1	0	0	1	1	V2
0	1	1	0	0	1	1	0	V3
0	1	1	0	1	1	0	0	-V1
0	0	1	1	0	0	1	1	-V2
0	1	1	0	1	0	0	1	-V3

The number of output phase voltage levels is m=2s+1, s being the number of dc sources. Multilevel inverters are used for applications like static var generation an interface with renewable energy sources and for battery based applications. The inverter can be used to regulate the power factor of current and voltage of the system. Cascaded inverters are ideal for usage of renewable energy sources with an ac grid. Cascaded inverters is used as a main traction drive in electric vehicles. The cascaded inverter serves as a rectifier or charger for the batteries of electric vehicles when connected to ac supply. The cascaded inverter acts like a rectifier during regenerative braking.

3. NEUTRAL POINT CLAMPED INVERTER:

In this inverter diode is used as a clamping device to clamp the dc bus voltage, so the output voltage can be achieved in steps. It is also known as "Neutral Point Clamped Multilevel Inverter(NPCMLI)"[3]. The clamping diode can be used for connecting the neutral point to the midpoint of the switching pairs of IGBT[14]. By using the multilevel inverter topologies for the NPC, usage of many switches is preferred. Due to these number of switches, switching loss may occur in the circuit. The number of capacitors can be connected in parallel with the sources. The voltage across each capacitor is $V_{dc}/2$ and the voltage stress will be limited to one capacitor voltage level $V_{dc}/2$ through diodes. The voltage stress across the switching devices is partial to V_{dc} using the diode. The availability of the inverter can be increased due to the capability, extending the operating range, adjustable power factor. It can also used for balancing the voltage by reducing the loss[5],[6]. The main advantage is to balance the neutral point voltage and reduce the harmonic content[11]. It is effective and reduce the production

cost. This can be achieved by increasing the power of the electrical equipments and the size of installation. It also used in high power motor drives and it can be operating at several KV and also used for large industrial application.

4. BASIC CIRCUIT CONFIGURATION (FOR SINGLE PHASE)

Figure.2 shows the configuration for the three level NPC inverter. The voltage across the switch is one half of the two level inverter. The IGBT's are connected in series. The voltage source is splitted into two by the clamping diodes to the neutral point.
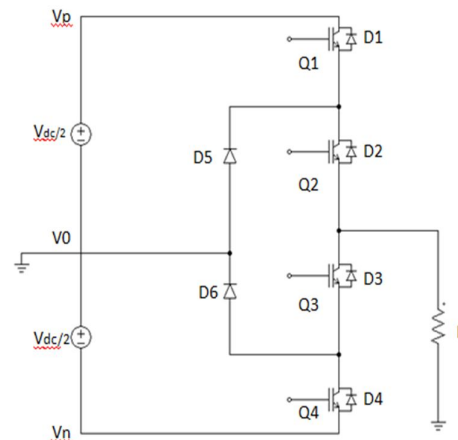

Fig.2.Three level NPC for single phase

### 5. OPERATION AND SWITCHING STATES

The NPC has three voltage levels: (1)Positive DC voltage, (2) zero voltage and (3) negative DC voltage. When the IGBT's Q1 and Q2 is turned on, the voltage is connected to V_p and reverses to the neutral point through diode D5 When the IGBT's Q2 and Q3 is turned on, the voltage can be at Vo. When the IGBT's Q3 and Q4 is turned on, the voltage can be connected to V_n and reverses to the neutral point through the diode D6. But the IGBT's Q2 and Q3 results in more conduction loss and for less switching loss. The diode which is parallel with the IGBT is on, thus for holding the recovery voltage across the diode to the IGBT Vc. The switching states for three level inverter can be shown in table 1.

Table 2: Switching States for NPC

| IGBT	V0=Vp	V0=Vo	V0=Vn
Q1	on	off	off
Q2	on	on	off
Q3	off	on	on
Q4	off	off	on

6. MULTIBAND HYSTERESIS MODULATION

The graphical representation for multiband hysteresis modulation is shown in fig 1. The basic building block for cascaded H bridge inverter is shown. The switches IGBT with an antiparallel diode. Cascaded H bridge inverter require N=(n-1)/2 H bridges. Voltage and power stress is distributed among the switches. The output voltage of n level inverter is V0= uVdc. The voltage stress on the semiconductor switches and the dc link voltage is 1/N times the net dc link voltage Vdc for n level inverter. The generalised multiband hysteresis modulation tracks the desired reference current in the load side in current controlled operation mode h – net hysteresis band, – dead zone introduced to prevent overlapping between loops. The inverter is made to track the desired output current i to reference value i ref. Multiband hysteresis controller modulates the signal with N number of bands and compares the current error e=(iref –i) with sector based hysteresis bands h and switching signals are generated for the power switches S11,S12,…..SN4 of the various H bridges of the inverter.
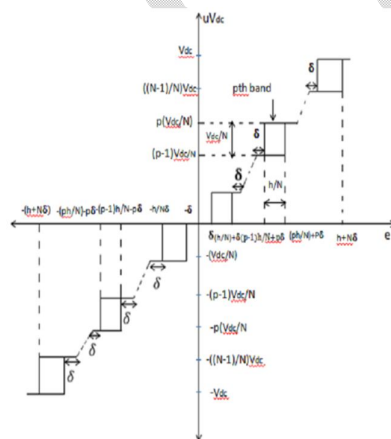
Fig 3:Generalised multiband hysteresis modulation for N level inverter

The multiband hysteresis modulation scheme for the multilevel inverters uses symmetrical hysteresis bands called upper band and lower band to control the switching over to the adjacent level. When the error signal crosses the inner boundary level 1,the output of the inverter is increased or decreased by one level depending on the upper or lower boundary limit which it has crossed.

The change in the voltage level will cause current error (e) to reverse its direction within the band limit to track its own path before reaching the next higher boundary limit. If the error does not reverse its direction then the error may reach the immediate next boundary limit(outer boundary 2). At the next higher boundary limit the next voltage level of multilevel inverter will be switched. This process continues only till the current error reverses. The voltage level applied at the each boundary level of the current error should be sufficient enough to force the current error back within the respective bandlimit.
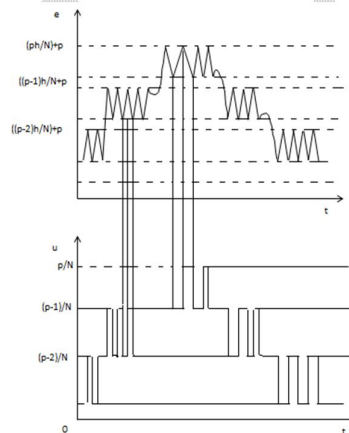
Fig.4Tracking error characteristics in various hysteresis bands

GENERALISED SWITCHING ALGORITHM:

Let us consider that the five level inverter is operating in the pth band. The Hysteresis band starts from [(p-1)h/N+p] and ends at [ph/N+p] level for the pth band corresponding to the (p-1)Vdc/N and pVdc/N voltage levels. The length of the net effective hysteresis band is h/N and voltage Vdc/N is the difference between the net operating voltage level for the particular band. The voltage levels (p-1)Vdc/N and pVdc/N is the output for the switching algorithm.

GENERALISEDDERIVATION OF SWITCHING FREQUENCY:

The time domain representation of the current tracking error e(t) The time-domain representation of the current tracking error e(t) and corresponding switching logic u(t) for positive half cycle using the multiband hysteresis algorithm. When the current error e touches the hysteresis band limit $((p–1)h/N+ p\delta))$ before start of the duration t1 , then the switch $Sp3$ gets turned ON and u=(p–1)/Nin the interval $t1$, satisfying the switching algorithm condition

ii-(b) for positive half cycle given in Table I for the condition "Ife $<((p–1)h/N+ p\delta)$." As a result the actual current (i−) starts to decay with the negative slope until the increasing current error e+ exceeds the upper hysteresis band limit (ph/N+ pδ), before the start of duration t2 . After which the switch Sp2 gets turned ON and u = p/Nin the interval t2 , satisfying the switching algorithm condition ii-(b) for the condition

As a result the current (i+) starts to increase with the positive slope until the decreasing current error (e−)crosses the lower hysteresis band limit $((p–1)h/N +p\delta)$.
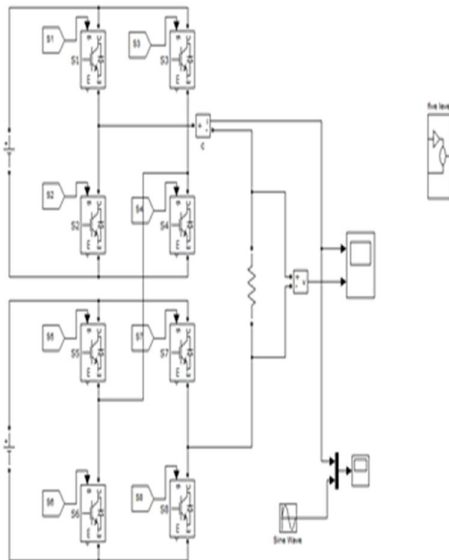
SIMULATION DIAGRAM:

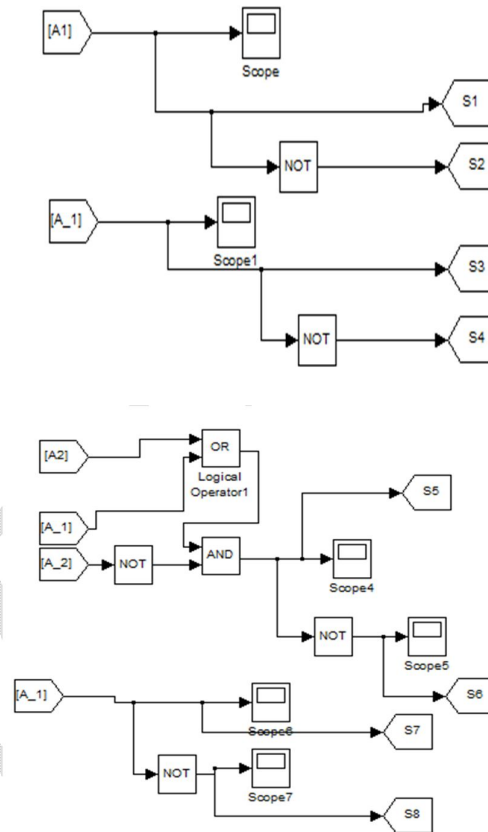Fig 5 :Simulation model for five level inverter

Fig 6:Simulation model for pulse generation.
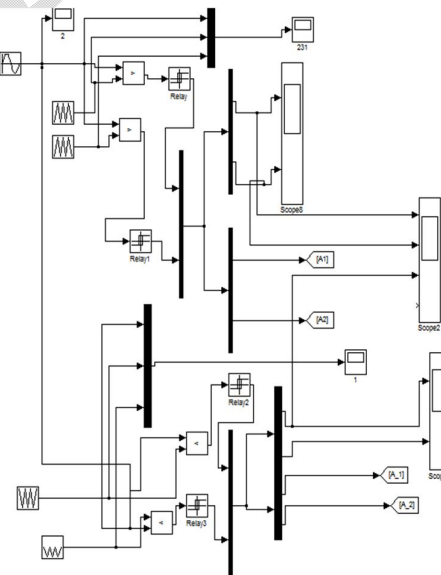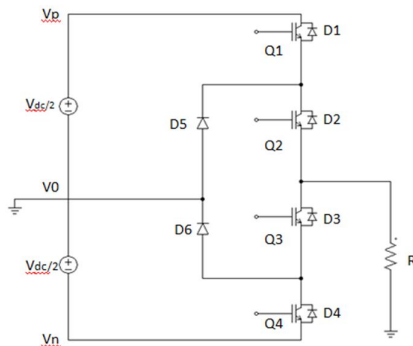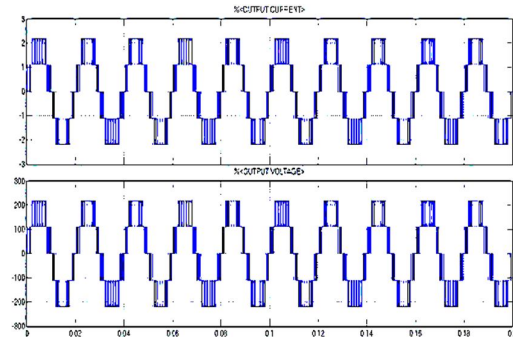

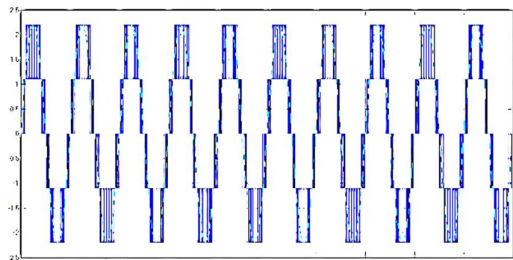**Fig 7:Multiband hysteresis modulation Simulink model**
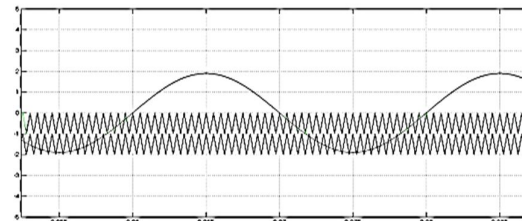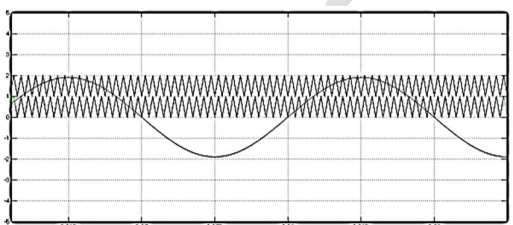
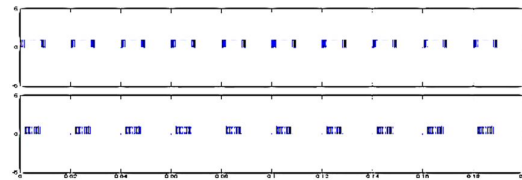**Fig.8.Three level NPC for single phase**
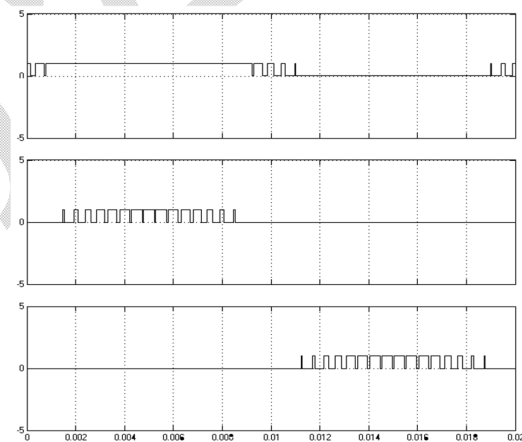
SIMULATION RESULTS:

(a)5 level CMLI inverter

(b)comparison waveform

(c)Multiband hysteresis modulation for CMLI
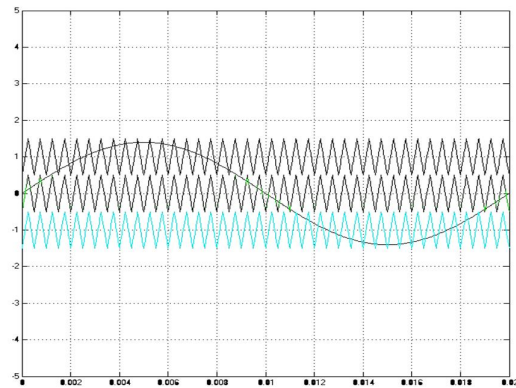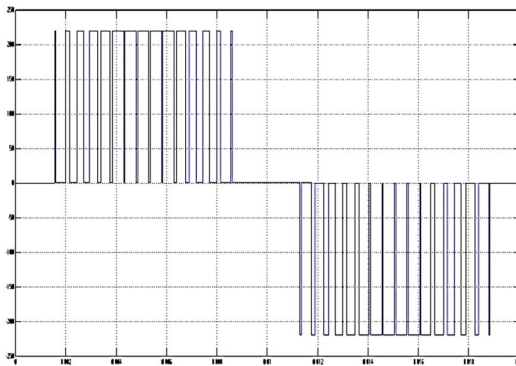

(d)Pulse generation for CMLI

(e)Pulse generation for NPC

(f)Multiband hysteresis modulation for NPC

(g)3 level npc inverter

Simulation studies are performed on the single phase grid connected H bridge multilevel inverter using MATLAB simulation software. The system parameters are h-net hysteresis band is the dead zone for the desired maximum switching frequency the system parameters are given in table II. The value of net hysteresis band is calculated for the desired maximum switching frequency. The deadband of this modulation is about 10-15% of the hysteresis bandwidth. The calculated hysteresis band is used for deriving the instantaneous, minimum and maximum switching frequency. The average switching frequency is calculated over one cycle of power frequency. The inverter switching losses and total harmonic distortion of current can be estimated for a given switching frequency.

The estimation of the switching losses and source current distortions is used for the calculation of different average instantaneous switching frequency by varying the value of the band limits. On the basis of of various observations 2.0 khz is selected as effective maximum switching frequency for the switches to operate with low switching losses and low supply current distortions to to be less than 5%.The value of the hysteresis band for fcmax of 2.0 khz is calculated using h=5.2A.The dead zone of the

band = 0.65 is chosen such that it is about 12% of hysteresis bandwidth h. The simulation of the five level inverter with multiband hysteresis modulation technique is done successfully. Simulation results show that the five level inverter switches operate at fundamental switching frequency. Harmonics in the inverter are less. The simulation results are almost same as the predictions.

7. CONCLUSION

This paper is the study of a multiband hysteresis control technique based on time domain formulation for cascaded H bridge multilevel inverter and Neutral point clamped multilevel inverter. The generalised switching frequency in time domain formulation is used for the design of multiband hysteresis controller for tracking the desired reference current and to track the error signal for the inverters within the band range. The simulation results are obtained for five level cascaded H bridge multilevel inverter using multiband hysteresis controller. The results are useful in determining the total switching losses ,total harmonic distortions and the efficiency of the controller's operation.

FUTURE WORK:

The work presented here is just the multiband hysteresis modulation technique for Cascaded H bridge 5 level inverter and neutral point clamped inverter. The design of these inverters as filter DVR will be useful to improve the power quality. The Simulink model of these inverters can be used for the design of DVR.

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